

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (withdrawn): A semiconductor device, comprising:

 a gate oxide located over a substrate; and

 a silicided gate electrode located over said gate oxide, said silicided gate electrode including a first metal and a second metal.

Claim 2 (withdrawn): The semiconductor device as recited in Claim 1 further including a dopant located within and configured to tune a work function of said silicided gate electrode.

Claim 3 (withdrawn): The semiconductor device as recited in Claim 2 wherein said dopant is selected from a group consisting of:

 boron;

 phosphorous; and

 arsenic.

Claim 4 (withdrawn): The semiconductor device as recited in Claim 1 further including source/drain regions located in said substrate proximate said gate oxide and silicided source/drain contact regions located in said source/drain regions, wherein said silicided source/drain contact regions have a depth substantially different than a thickness of said silicided gate electrode.

Claim 5 (withdrawn): The semiconductor device as recited in Claim 4 wherein said silicided gate electrode is silicided with a different metal than said silicided source/drain contact regions.

Claim 6 (withdrawn): The semiconductor device as recited in Claim 1 wherein said first metal is cobalt and said second metal is nickel.

Claim 7 (withdrawn): The semiconductor device as recited in Claim 6 wherein a ratio of an atomic percent of said cobalt to said nickel in said silicided gate electrode ranges from about 9:1 to about 2:3.

Claim 8 (withdrawn): The semiconductor device as recited in Claim 7 wherein said atomic percent ranges from about 3:1 to about 1:1.

Claim 9 (withdrawn): The semiconductor device as recited in Claim 1 wherein said silicided gate electrode has a thickness ranging from about 15 nm to about 150 nm.

Claim 10 (currently amended): A method for manufacturing a semiconductor device, comprising:

placing a blanket layer of gate oxide material over a substrate; and

forming a silicided gate electrode over said gate oxide including;

forming a blanket layer of polysilicon material over said blanket layer of gate oxide material;

forming a blanket layer of an alloy comprising a first metal and a second metal over said blanket layer of polysilicon material; and

implanting a dopant into said blanket layer of polysilicon material affecting a work function of said silicided gate electrode; and

annealing said blanker layer of said alloy comprising said first metal and said second metal to form a blanket layer of silicided gate electrode material including said first metal and said second metal.

Claim 11 (canceled)

Claim 12 (currently amended): The method as recited in Claim 10 further including patterning said blanket layer of silicided gate electrode material to form said silicided gate electrode including said first and said second metals.

Claim 13 (currently canceled):

Claim 14 (currently amended): The method as recited in Claim 10 13 further including forming a capping layer over said blanket layer of said alloy, said capping layer configured to affect a doping profile of said dopant.

Claim 15 (original): The method as recited in Claim 14 wherein said capping layer comprises a transition metal-nitride.

Claim 16 (canceled)

Claim 17 (withdrawn): The method as recited in Claim 11 wherein said cobalt -nickel alloy has a Co_x to Ni_y ratio (x:y) ranging from about 9:1 to about 2:3.

Claim 18 (previously presented): The method as recited in Claim 10 wherein a ratio of an atomic percent of said first metal to said second metal in said silicided gate electrode ranges from about 9:1 to about 2:3.

Claim 19 (original): The method as recited in Claim 10 further including forming source/drain regions in said substrate and forming silicided source/drain contact regions in said source/drain regions subsequent to forming said silicided gate electrode.

Claim 20 (withdrawn): An integrated circuit, comprising:

transistors located over a substrate, said transistors including;
a gate oxide located over said substrate;
a silicided gate electrode located over said gate oxide, said silicided gate electrode including a first metal and a second metal; and
an interlevel dielectric layer located over said substrate, said interlevel dielectric layer having interconnects located therein for contacting said transistors.

Claim 21 (previously presented): The method as recited in Claim 18 wherein said first metal is cobalt and said second metal is nickel.

Claim 22 (previously presented): The method as recited in Claim 10 wherein said first metal is cobalt and said second metal is nickel.